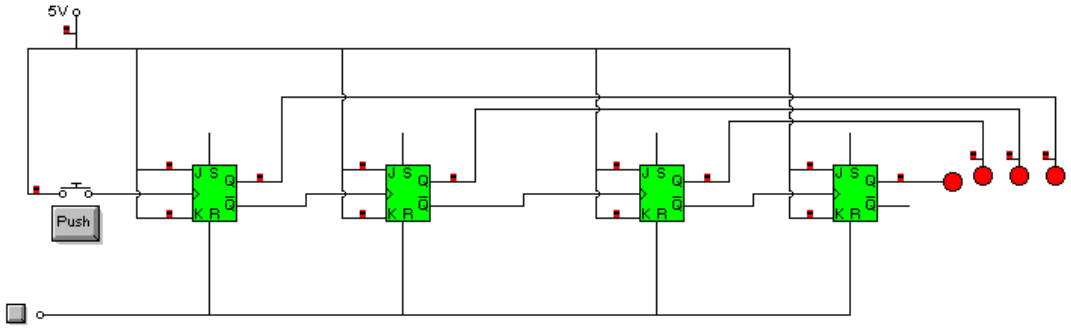
# JK Flip-Flop Counter Circuits

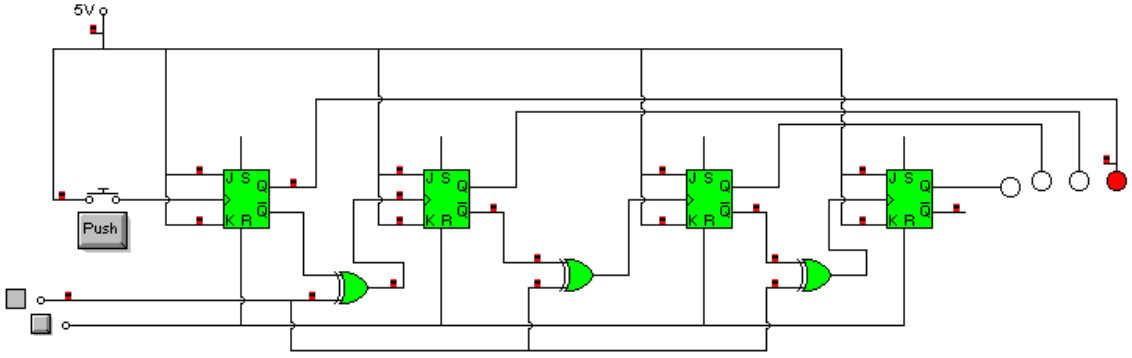
1. Construct the following circuit in Crocodile Physics. Note that the change in the second flip-flop is triggered by the output of the first flip-flop. Because the flip-flops do not all change state at the same time, this is known as an asynchronous or ripple counter. If you turn the R inputs high, and then low again, what happens to the counter? After resetting the counter, push the button 16 times and record the output as binary numbers.




| Pulse | DC BA |
|---|---|
| <Reset> | 0 0 0 0 |
| 1 | |
| 2 | |
| 3 | |
| 4 | |
| 5 | |
| 6 | |
| 7 | |
| 8 | |

| Pulse | DC BA |
|---|---|
| 9 | |
| 10 | |
| 11 | |
| 12 | |
| 13 | |
| 14 | |
| 15 | |
| 16 | |

2. The circuit above counts only in one direction—up. The circuit below will count up or down depending on the state of the third input switch.




Analyse the truth tables and explain why the addition of XOR gates can change the direction in which the counter operates. _____

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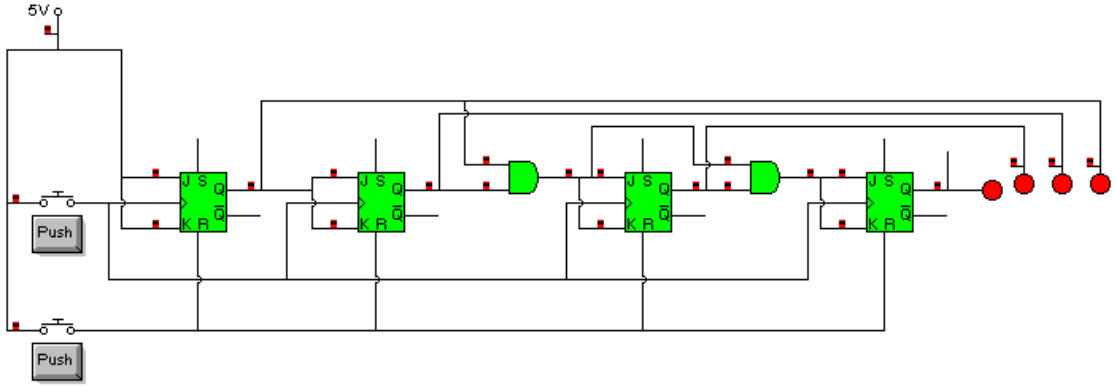
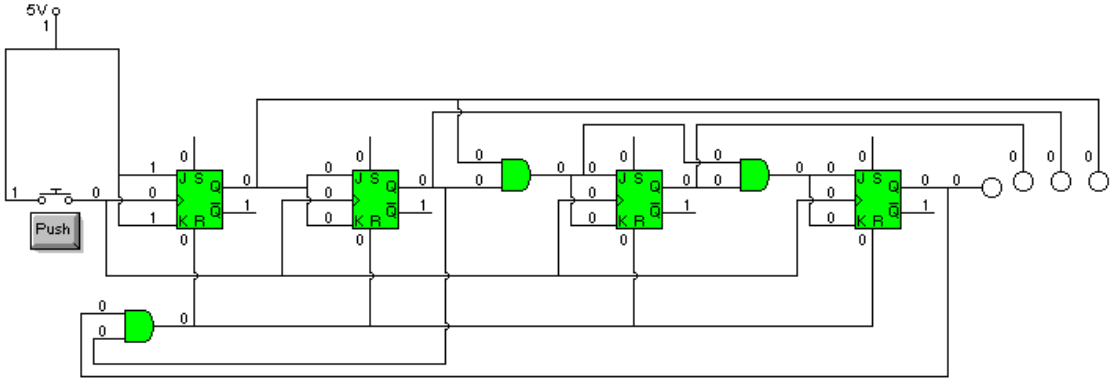
3. In applications where fast responses are required, the built-in delays of a ripple counter are unacceptable. A synchronous counter is one in which the input clock pulse is connected to all the flip-flops so they all operate at the same time. This requires the addition of logic gates to control when each flip-flop toggles.




Build the circuit above, and observe it carefully in operation. Since the clock is connected directly to the clock input on all the Flip-Flops, why don't they all toggle on every clock pulse? (Refer to the truth table for the J-K Flip-Flop)

4. With four bits, a counter can count from 0 to 16. Sometimes it is desirable to have the counter stop counting at some other value. In the circuit below, the reset input has been used to turn the 0-to-15 binary counter into a decimal 0-to-9 counter.




Why does this counter reset itself after the count of 9?

What changes would you make to this circuit to cause it to reset after the count of 6?