Integrated Circuit Logic Gates

Objective: Students will be able to construct Logic Circuits using Integrated Circuits.

In this activity you will use integrated circuit logic chips to build networks of logic gates.

The chips you will use are from the 74xxx series of chips. These chips come in a package known as DIP (Dual In-line Package) because the plastic container has two parallel rows of pins to connect the inner circuits to a circuit board. Inside the package are networks of transistors designed to perform a wide variety of functions. Each chip is labeled with a number which indicates what the function of the chip is. Pin 1 is marked by a small circular indent or a U-shaped indent atone end of the chip; the remaining pins are numbered counterclockwise around the chip.

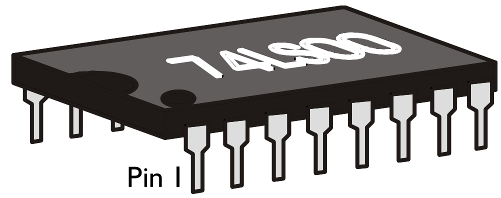


Fig. 1: DIP Package

The 7400 chip, for example, contains four 2-input NAND gates, but chips are available with all types of logic gates, timers, counters, adders and subtractors, encoders and decoders, and memory, to name a few. In fact in the late sixties and early seventies, entire computers were built by soldering thousands of these chips together on circuit boards. They are still in use today in electronic devices where the power of a complete microprocessor is not needed.

The 74xxx series of chips use bipolar transistors in a type of circuit known as Transistor-Transistor Logic (TTL). While MOS and CMOS technologies are more compact and energy efficient than TTL, they are easily damaged by static electricity. TTL circuits operate with 5 Volts DC power. Each chip must have the common or negative connected to the Ground (GND) pin, and +5 volts connected to the pin marked Vcc (Common Collector Voltage).

The numbers on the chips also provide other information about the contents of the package: The number is usually in the format MM74TTXX in which MM is the Manufacturer's code, TT is the type of circuit and XX is the function of the chip. LS for example stands for a type of circuit known as Low Power Schottky, which uses Schottky diodes to improve the performance of the circuitry.

The diagram at right is the logic diagram for the 7400 chip which contains four 2-input NAND gates. Note the power connections on pins 7 and 14. Pins 1 and 2 are the inputs for the first NAND gate, and the output is on pin 3. Logical 0 is represented by a voltage at or near 0V, while logical 1 is represented by a voltage close to 5 volts (a minimum of 2.7 volts). In this activity, you will monitor the state of the inputs and outputs by connecting them to LED indicator lights. When the light is on it indicates that the voltage is high, and when it is off the voltage is low.

74LS00
Quad 2-Input
NAND Gate

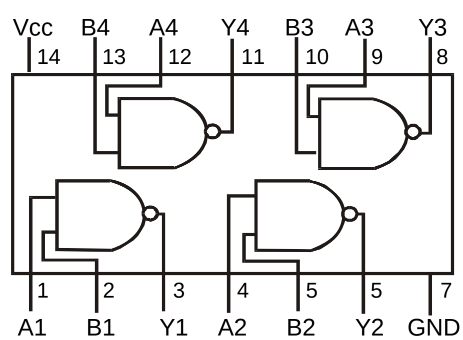
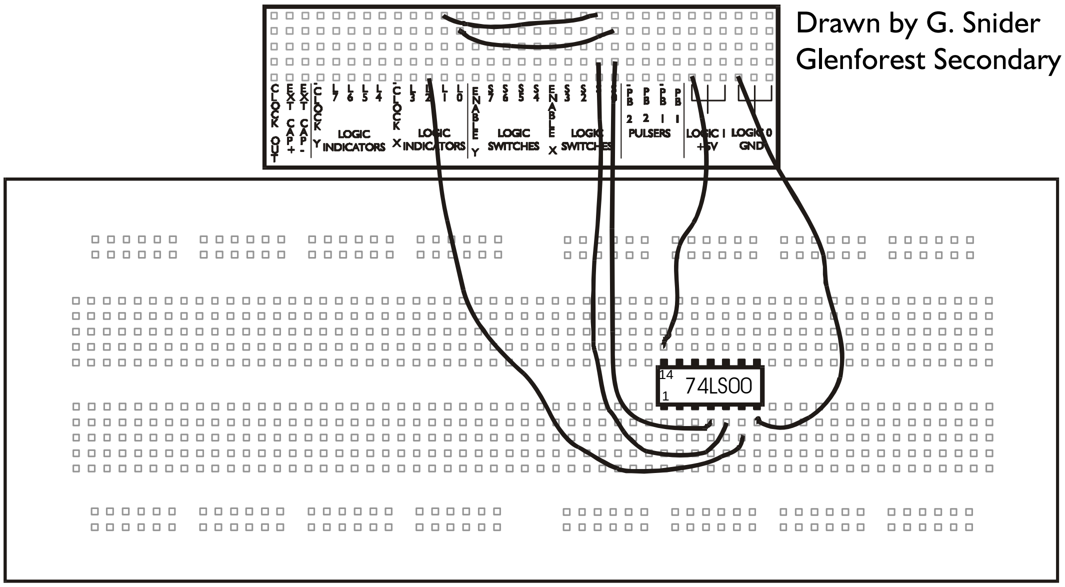


Fig. 2

Procedure

1. You will build your circuit on the PencilBox Logic Trainer. The PencilBox has built-in features that make building and testing IC logic circuits quite simple. The larger of the two breadboards is where you will build your circuit. The sockets on the smaller breadboard are connected by the printed circuit board to the buttons, switches and LEDs mounted on the board. To connect your circuit for power, for example, you use the section of the small breadboard with the connectors labeled **Logic 1(+5V)** and **Logic 0 (GND)**.



Drawn by G. Snider
Glenforest Secondary School

2. Before you begin to build your circuit, make sure that the power to the PencilBox is off.
3. Plug the 74LS00 IC into the main breadboard so that it straddles the centre divider. Plugging it in anywhere else on the board will short-circuit the opposite pins.
4. Insert a wire next to pin 7 and connect it to the negative side of the power supply (Logic 0). Insert a second wire next to pin 14 and connect it to + 5V.
5. Connect a wire from pin 6 on the 7400 chip to a point on the smaller breadboard labeled L2. This connects the output of the NAND gate to the third LED indicator light.
6. Connect pin 4 to S0 and connect pin 5 to S1. This will connect the inputs of the NAND gate to the Logic Switches – the small rocker switches contained in a package the same size as the 7400 chip. (These switches are known as DIP switches because of the packaging.)
7. Connect the power supply to the socket on the PencilBox and turn on the switch.
8. Turn both of the Logic Switches off, so that L0 and L1 are both off. L2 should now be on if your circuit is working correctly.
9. Turn the switches on one at a time, and then turn on both. Observe whether the output (L2) is on or off. Record the results in the form of a truth table on the answer sheet. Does the truth table correspond to the NAND gate?
10. Turn off the PencilBox and add wires to the circuit to produce the circuit shown in *Fig 4.* Following the same procedure as above, construct a truth table for this combination of gates, in which the inputs are on pins 9 and 10 and the output is still connected to pin 6. Record the results on the answer sheet and identify the gate which this circuit mimics.

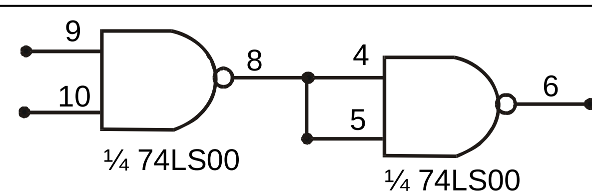


Fig. 4

11. Being sure to disconnect the power before you change the circuit, add more wires to produce the circuit shown in *Fig 5.* Following the same procedure as above, construct a truth table for this combination of gates, in which one inputs is on pin 9 or10, the second input is on pin 1 or 2 and the output is still connected to pin 6. Record the results on the answer sheet and identify the gate represented by this circuit.

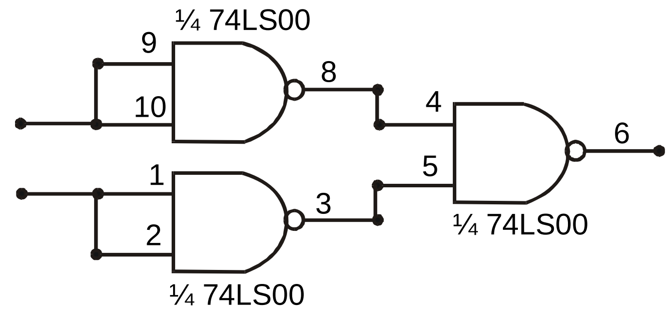


Fig 5

12. The next circuit requires the use of all the gates available on the 74LS00 IC. Once again, observe the output of the circuit with all possible combinations of inputs, and record the results on the answer sheet.

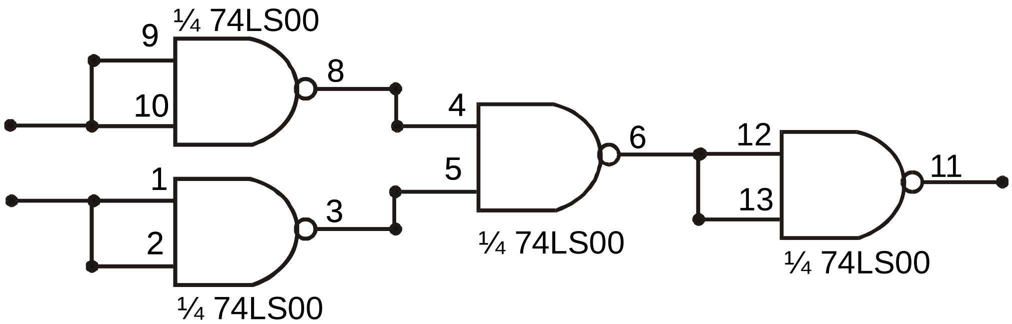


Fig. 6

13. The final circuit requires the addition of another IC, the 74LS04. This chip is described as a Hex Inverter IC because it contains six NOT gates. Plug the new chip into the board so that it straddles the centre divider. Once again, power must be connected to pins 7 and 14. The pin numbers for the inputs and outputs of the required inverters are shown on the diagram. As before, construct a truth table and identify the gate.

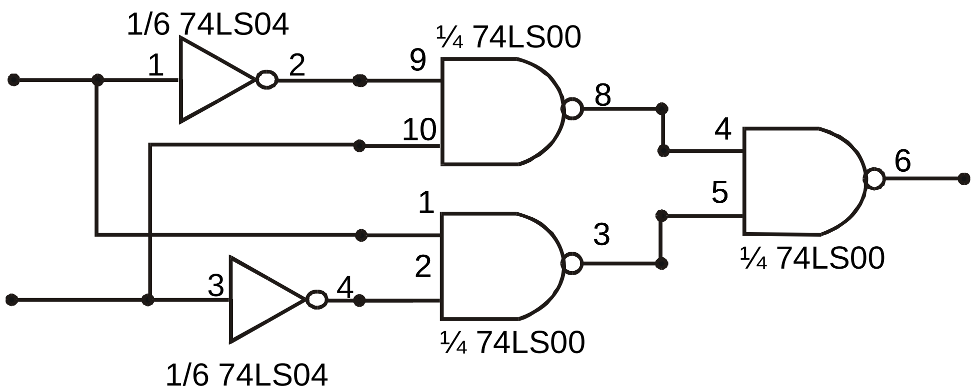
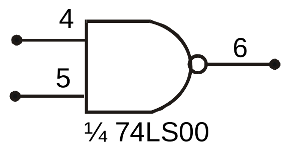


Fig. 7

Answer Sheet: IC Logic Gates

8. Gate: ________________

A	B	*y*
L	L	
L	H	
H	L	
H	H	



9. Gate: ________________

A	B	*y*
L	L	
L	H	
H	L	
H	H	

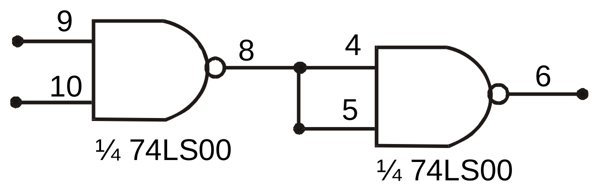


Fig. 4

10. Gate: ________________

A	B	*y*
0	0	
0	I	
I	0	
I	I	

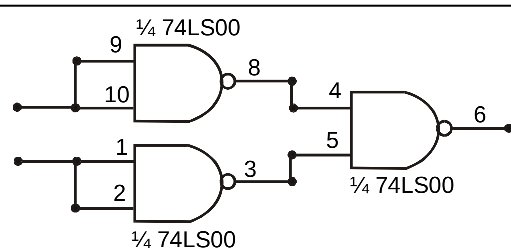


Fig 5

11. Gate: ________________

A	B	*y*
0	0	
0	I	
I	0	
I	I	

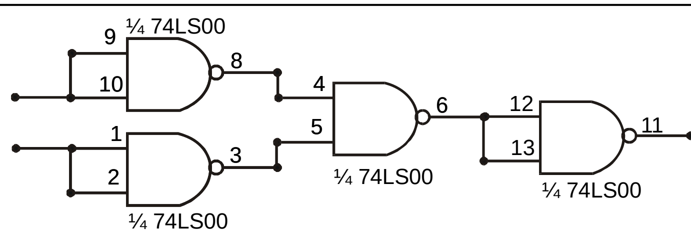


Fig. 6

12. Gate: ________________

A	B	*y*
0	0	
0	I	
I	0	
I	I	

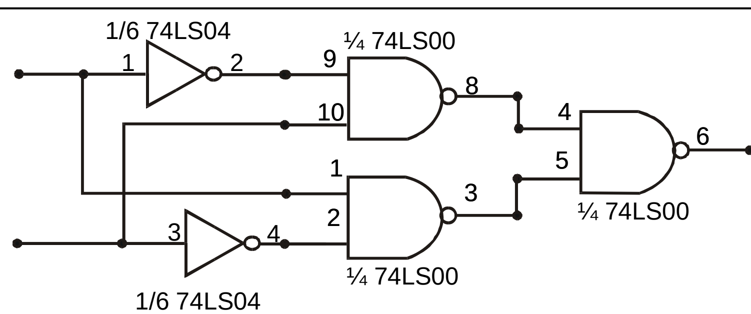


Fig. 7